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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/070,653	07/22/2002	Richard Spitz	10191/2277	9239
26646	7590	08/25/2004	EXAMINER	
KENYON & KENYON ONE BROADWAY NEW YORK, NY 10004			MONDT, JOHANNES P	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

km

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/070,653	SPITZ, RICHARD	
	<b>Examiner</b>	<b>Art Unit</b>	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06 July 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 9-14 and 16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 9-14 and 16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/06/2004 has been entered.

### ***Response to Amendment***

Amendment filed with aforementioned Request for Continued Examination forms the basis for this Official Action. In said Amendment Applicant substantially amended claims 9-14 and 16 through substantial amendment of claims 9 and 16. Claim 15 was canceled. Claims 9-14 and 16 are in the application, claims 1-8 having been canceled previously.

Comments on Remarks in said Amendment are included below under "Response to Arguments".

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. ***Claims 9-14 and 16*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Through independent claims 9 and

16, all claims contain subject matter not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. In particular, the wording "applying metal layers" (claim 9, final line, and claim 16, final line) has not been disclosed. Instead, only the coating with metal layers (page 3, lines 10-21 of the Specification) is disclosed, which is a concept fully contained in and narrower than the concept of metallization (see Merriam-Webster's Collegiate Dictionary, tenth Edition, p. 730), which is the coating, treating or combining with a metal, while the application of a metal layer also includes the case in which the object and the metal layer do not have a single common interface, as is the case with coating.

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. **Claims 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over Henry et al (FR 75-24147 (Application Number)) in view of Goodrich et al (5,343,070). The present art rejection is provided with reference to the rejection based on 35 U.S.C. 112, first paragraph given above because of the introduction of new matter.

*Henry et al teach* a semiconductor component (cf. title and page 1, l. 1-10) comprising: a first layer 2 (cf. page 2, l. 26-30 and page 4, l. 5-7, from the latter it is

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evident that p- is an alternative to i-type for region 2) of a first conductivity type (lightly doped, p- type) having a top side and a bottom side, the first layer having areas of different thickness due to at least one depression 111 (and 112 cf. page 3, l. 6-14) introduced into the top side; a second layer 3 (cf. page 2, l. 26-30) of a second conductivity type (n+ type) covering the top side of the first layer; and a third layer 1 situated on the bottom of the first layer (cf. page 2, l. 26-30), wherein the first, second and third layers are diced into individual chips (along 21 and 23) (cf. Figure 1) (cf. page 2, l. 22-30), so that, in an internal area, each of the chips has at least one depression 111 or 112; wherein the depressions are sawed (cf. page 1, l. 36 – page 2, l. 3); and applying metal layers to a first layer 30 and a third layer of the wafer opposite said first layer through the process of metallization (cf. page 3, l. 6-14) (N.B.: The Specification of Applicant discloses coating with metal, see page 3, lines 10-21, and Figure 3a: in particular, providing metallic coating of layers 20 and 80), while the wording “applying metal layers to” has not been separately disclosed (see rejections under 35 U.S.C. 112, first paragraph, above) (see page 3, l. 11-21). Because Henry et al teach metallization of the *surfaces* of first and third metal layers (respectively applied to surface 30 and to the surface opposite to 30; see page 3, lines 6-14) it must be stated that Henry et al teach the *coating* of said first and third metal layers *with metal*, i.e., teach the application of metal layers, namely the coatings, to the first and third layers as disclosed by Applicant.

*Henry et al do not necessarily teach* the limitation that said depression to be sawed in an internal area such that none of the first layer, second layer and third layer

include edge areas that have depressions. *However, it would have been obvious* to include said limitation in view of Goodrich et al, who teach a mesa type PIN diode (cf. title) and a method of making mesa type PIN diodes (cf. abstract) wherein the depressions 24 (cf. Figures 2, 4 and 16; col. 8, l. 66 – col. 9, l. 5) are to be kept away from the edge areas by a distance 27 at least twice the (finite) thickness of the thickness of the intrinsic region 16 for the specific purpose of enhancing the advantageous characteristics of the diode 10 by causing the device current to be away from the sidewalls and their trap levels, thereby greatly reducing Shockley-Read-Hall charge carrier recombination effects detrimental to the charge that can be stored in the device (cf. col. 2, l. 4-22, col. 2, l. 42-61). *Motivation* to include the teaching by Goodrich et al in the device by Henry et al is the consequent improvement of the amount of charge storable in the PIN diode. *Combination* of the teaching by Goodrich et al with the device by Henry et al merely involves a selection of the lines of sawing. Success in implementing the combination can therefore be reasonably expected.

3. ***Claims 9-10 and 12-14*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Henry et al (FR 75 24147) in view of Rummenik (4,220,963) and Goodrich et al (5,343,070). Henry et al teach a method of manufacturing semiconductor components (cf. title) comprising: introducing depressions 111 and 112 (cf. page 2, l. 15-21) into a wafer 1/2 (cf. page 2, l. 26-30; see also page 4, l. 5-7) of first conductivity type (N-type); coating both sides of the wafer with doping atoms (to peripheral regions 1 and 3 on both sides of the wafer) by carrying out a diffusion process (cf. page 1, l. 30-

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37) (yielding heavily doped peripheral regions 1 and 3 (cf. Figures 2 and 3; cf. page 2, l. 26-30)); dicing the wafer into individual chips (cf. page 5, l. 7-10 and Figure 1) in such a way that, in an internal area, each of the chips has at least one depression (cf. Figures 1 and 3), said depressions being an essential part of the device; wherein the depressions are sawed (cf. page 1, l. 36 – page 2, l. 3); and applying metal layers to a first layer 30 and a third layer of the wafer opposite said first layer through the process of metallization (cf. page 3, l. 6-14) (N.B.: The Specification of Applicant discloses coating with metal (see page 3, lines 10-21, and Figure 3a: in particular, providing metallic coating of layers 20 and 80). The term “applying metal layers to” as such does not occur in the Specification; please note that instead doped layers are applied, which then are given a metallic coating (see page 3, l. 11-21). Because Henry et al teach metallization of the *surfaces* of first and third metal layers (respectively applied to surface 30 and to the surface opposite to 30; see page 3, lines 6-14) it must be stated that Henry et al teach the *coating* of said first and third metal layers *with metal*, i.e., teach the application of metal layers, namely the coatings, to the first and third layers as disclosed by Applicant.

*Henry et al do not necessarily teach* the further limitation that the method with which the doping atoms are introduced to peripheral regions 1 and 3 comprises the steps of coating both sides of the wafer with said doping atoms and carrying out a diffusion process. *However, it would have been obvious to include* said further limitation in view of Rummenik, who teaches in a patent on a fast recovery diode, hence analogous art, the use of diffusion doping to create desired doped peripheral regions 11

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and 12 on opposite sides of the wafer (cf. col. 2, l. 26-38). *Motivation* to include the method step taught by Rummenik in the method by Henry et al stems from the advantage that many wafers can be simultaneously subjected to diffusion doping through the use of a diffusion furnace. *Combination* of the teaching by Rummenik with the invention by Henry et al is straightforward through the use of the single heating step described by Rummenik (cf. col. 2, l. 26-38). Success in the implementation of said combination can therefore be reasonably expected.

*Henry et al do not necessarily teach* the limitation that said depression to be sawed in an internal area such that none of the first layer, second layer and third layer include edge areas that have depressions. *However, it would have been obvious* to include said limitation in view of Goodrich et al, who teach a mesa type PIN diode (cf. title) and a method of making mesa type PIN diodes (cf. abstract) wherein the depressions 24 (cf. Figures 2, 4 and 16; col. 8, l. 66 – col. 9, l. 5) are to be kept away from the edge areas by a distance 27 at least twice the (finite) thickness of the thickness of the intrinsic region 16 for the specific purpose of enhancing the advantageous characteristics of the diode 10 by causing the device current to be away from the sidewalls and their trap levels, thereby greatly reducing Shockley-Read-Hall charge carrier recombination effects detrimental to the charge that can be stored in the device (cf. col. 2, l. 4-22, col. 2, l. 42-61). *Motivation* to include the teaching by Goodrich et al in the device by Henry et al is the consequent improvement of the amount of charge storable in the PIN diode. *Combination* of the teaching by Goodrich et al with the device



by Henry et al merely involves a selection of the lines of sawing. Success in implementing the combination can therefore be reasonably expected.

*On claim 10:* the depressions 111/112 are formed as pits, having rectangular cross sections (cf. Figures 2 and 3).

*On claim 12:* the wafer according to the method by Henry et al is diced in areas where no depressions have been introduced (cf. page1, l. 37 – col. 2, l. 5).

*On claim 13:* the method by Henry further comprises the step covering a top side of the wafer using a dopant of second conductivity type (p+ type in Figure 2).

*On claim 14:* the method by Henry further comprises the step covering a bottom side of the wafer using a dopant of the first conductivity type (n+ type in Figure 2).

1. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over Henry et al, Rummenik and Goodrich et al as applied to claim 9 above, and further in view of Schmid et al (5,985,067), or, in the alternative over Henry et al in view of Rummenik and Goodrich et al as applied to claim 9. Although neither Henry et al nor Rummenik nor Goodrich et al necessarily disclose the further limitation of claim 11 it is inherent to a PIN diode as taught by Henry et al to have both front and back side metallization as otherwise no electrical utility is feasible; furthermore, with regard to the order of steps implied by the further limitation of claim 11, it would have been obvious to include said further limitation in view of Schmid et al, who, in a patent on a method to produce chips from a metallized wafer (cf. abstract), - hence analogous art, teaches face metallization strips 101-105 on a first main surface 112 of a wafer 100 and face metallization strips

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106-110 on a second main surface of said wafer 100 (cf. col. 8, l. 57-61), and a method of cutting the wafer that comprises the step of cutting the wafer 100 along the face metallization strips (cf. claim 5 of Schmid et al; cf. col. 9, l. 27-31; also see end result in Figure 3, with face metallization strips 130 and 131 (cf. col. 9, l. 58-61)).

*Motivation* to include the teaching by Schmid et al in the invention by Henry et al, Rummenik and Goodrich et al derives from the improved voltage distribution over the metallic components (cf. col. 3, l. 7-18). *Combination* of said teaching with said invention only requires following the same dicing technique followed by Schmid et al and in no way interferes with the remainder of the invention by Henry et al, Rummenik and Goodrich et al. *Success* of the implementation of said combination can therefore be reasonably expected.

*In the alternative rejection over merely* Henry et al, Rummenik and Goodrich et al, Applicant is reminded of Ex Part Rubin, 128 USPQ 440 (Bd. App. 1959) (Prior Art disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1930) (Selection of any order of mixing ingredients is *prima facie* obvious). Consequently, in view of the absence of any teaching in Applicant's disclosure as to the critical nature of the order in which the metallization and the cutting steps are to be performed the further limitation of claim 11 thus only reduces to the application of metal layers to both sides of the wafer, which is inherent in any PIN diode.

### ***Response to Arguments***

4. Applicant's arguments filed 07/06/2004 have been fully considered but they are not persuasive. Specifically, in response to Applicant's traverse based on the newly amended claim language, it is noted that to "metallize" means: to coat, treat, or combine with metal (e.g., Merriam-Webster's Collegiate Dictionary, tenth Edition, page 730). On the other hand, out of all possible forms of "applying metal layers" the Specification of Applicant only discloses providing a "metallic coating" (see page 3, lines 10-21, and Figure 3a: in particular, providing metallic coating of layers 20 and 80). No discussion in the Specification is included why "applying metal layers" is distinct, let alone why any distinction is critical to the invention. Thus it must be stated that (a), as discussed above under 35 U.S.C. 112, first paragraph, the newly introduced amendment to claims 9 and 16 constitutes new matter in that the wording is substantially broader than disclosed in the Specification including the original claims, and that (b) because Henry et al teach metallization of the *surfaces* of first and third layers (respectively applied to surface 30 and to the surface opposite to 30; see page 3, lines 6-14) Henry et al teach the *coating* of said first and third metal layers *with metal layers*, which is the only form of a process of applying metal layers disclosed by Applicant. In view of the above, new rejections on the same art must herewith be provided.

***Conclusion***

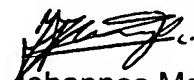
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM  
August 22, 2004

Patent Examiner:

  
Johannes Mondt  
Art Unit: 2826